appendix a CRC implementation

Although the requirement to perform multiple (modulo-2) divisions to compute a CRC may appear to be relatively complicated, in practice it can be done quite readily in either hardware or software. To illustrate this, a hardware implementation of the scheme used in Figure 6.22 is given in Figure A.1(a).

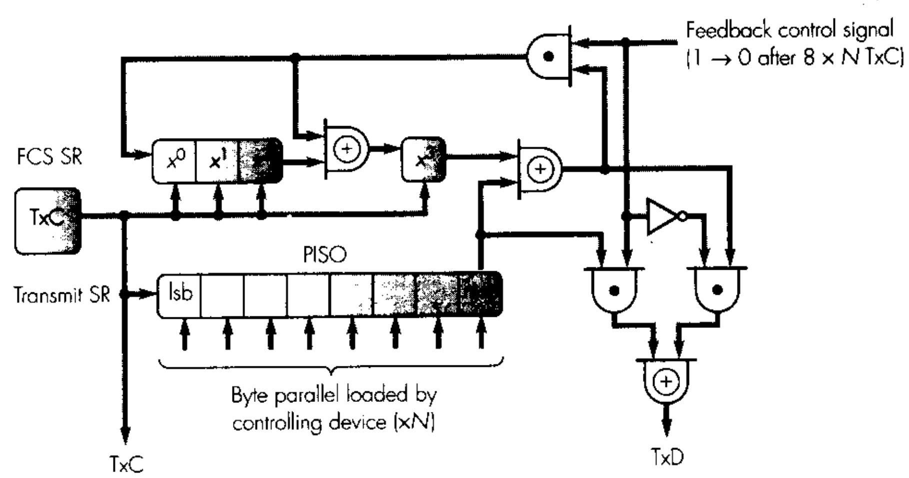
In this example, since we are to generate four FCS digits, we need only a 4-bit shift register to represent bits x^3, x^2, x^1, and x^0 in the generator polynomial. We often refer to these as the active bits of the generator. With this generator polynomial, digits x^3 and x^0 are binary 1 while digits x^2 and x^1 are binary 0. The new states of shift register elements x^1 and x^2 simply take on the states of x^0 and x^1 directly; the new states of elements x^0 and x^3 are determined by the state of the feedback path exclusive ORed with the preceding digit.

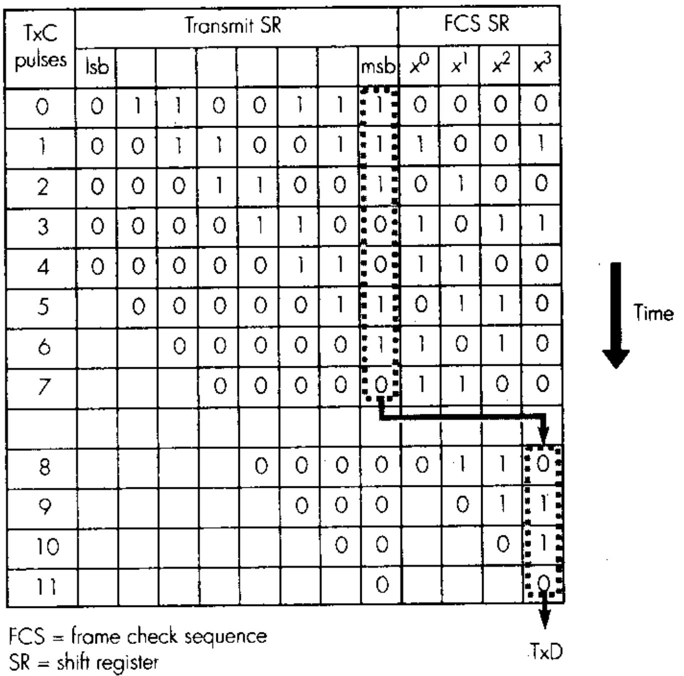
The circuit operates as follows. The FCS shift register is cleared and the first 8-bit byte in the frame is parallel-loaded into the PISO transmit shift register. This is then shifted out to the transmission line, most significant bit first, at a rate determined by the transmitter clock TxC. In time synchronism with this, the same bitstream is exclusive-ORed with x^3 and passed via the feedback path to the selected inputs of the FCS shift register. As each subsequent 8-bit byte is loaded into the transmit shift register and bit-serially transmitted to line, the procedure repeats. Finally, after the last byte in the frame has been output, the transmit shift register is loaded with zeros and the feedback control signal changes from 1 to 0 so that the current contents of the FCS shift register – the computed remainder – follow the frame contents onto the transmission line.

In Figure A.1(a) the contents of the transmit and FCS shift registers assume just a single-byte frame ($N = 1$), and hence correspond to the earlier example in Figure 6.22. In the figure the contents of both the transmit and FCS shift registers are shown after each shift (transmit clock) pulse. The transmitted bitstream is as shown in the hashed boxes.

The corresponding receiver hardware is similar to that used at the transmitter, as shown in Figure A.1(b). The received data (RxD) is sampled (shifted) into the SIPO receive shift register in the centre (or later with Manchester encoding) of the bit cell. Also, as before, in time synchronization with this the bitstream is exclusive-ORed with x^3 and fed into the FCS shift register. As each 8-bit byte is received, it is read by the controlling device. Again, the contents shown are for a frame comprising just a single byte of data.

(a)



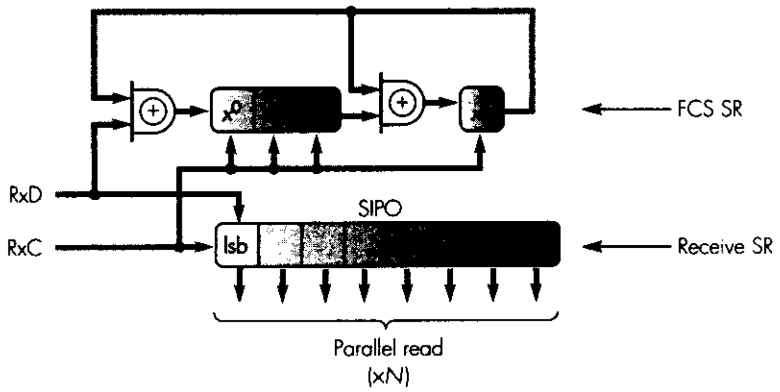


TxC pulses	Transmit SR								FCS SR			
	lsb							msb	x^0	x^1	x^2	x^3
0	0	1	1	0	0	1	1	1	0	0	0	0
1	0	0	1	1	0	0	1	1	1	0	0	1
2	0	0	0	1	1	0	0	1	0	1	0	0
3	0	0	0	0	1	1	0	0	1	0	1	1
4	0	0	0	0	0	1	1	0	1	1	0	0
5		0	0	0	0	0	1	1	0	1	1	0
6			0	0	0	0	0	1	1	0	1	0
7				0	0	0	0	0	1	1	0	0
8					0	0	0	0	0	1	1	0
9						0	0	0		0	1	1
10							0	0			0	1
11								0				0

FCS = frame check sequence
SR = shift register
PISO = parallel-in, serial-out

Figure A.1 CRC hardware implementation schematic: (a) CRC generation; (b) CRC checking.

(b)



RxC	RxD	Receive SR (shift register)								FCS SR			
		lsb							msb	x^0	x^1	x^2	x^3
0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1								1	0	0	0
2	1	1	1							1	1	0	0
3	0	1	1	1						1	1	1	0
4	0	0	1	1	1					0	1	1	1
5	1	0	0	1	1	1				1	0	1	0
6	1	1	0	0	1	1	1			1	1	0	1
7	0	1	1	0	0	1	1	1		0	1	1	1
8	0	0	1	1	0	0	1	1	1	1	0	1	0
		Byte read by controlling device											
9	1									0	1	0	1
10	1									0	0	1	1
11	0									0	0	0	0
12										0	0	0	0

Time ↓

SIPO = serial-in, parallel-out

Remainder = 0

Figure A.1 Continued.

The hardware in Figure A.1 is normally incorporated into the transmission control circuits associated with bit-oriented transmission. In some instances, however, a CRC is used in preference to a block sum check with character-oriented transmission. In such cases, the CRC must normally be generated in software by the controlling device rather than in hardware. This is relatively straightforward as we can see from the pseudocode in Figure A.2.

```
{Assume a preformatted frame to be transmitted (including a zero byte at its tail) or a received frame
is stored in a byte array buff[1.. count]. Also that the 8 active bits of a 9-bit divisor are stored in the
most-significant 8 bits of a 16-bit integer CRCDIV. The following function will compute and return the
8-bit CRC}

function  CRC : byte;
var       i, j : integer;
          data : integer

begin     data := buff[1] shl 8;
          for j := 2 to count do
               begin
                    data := data + buff [j];
                    for i := 1 to 8 do
                         if ((data and $8000) = $8000) then
                         begin data := data shl1;
                                data := data xor CRCDIV; end
                         else   data := data shl 1;
               end;

          CRC := data shr 8;
end;
```

Figure A.2 Pseudocode for the computation and checking of an 8-bit CRC.

The code assumes an 8-bit generator polynomial (divisor) and that the preformatted frame – STX, ETX, and so on – is stored in an array. The same code can be used for CRC generation and checking; for generation the array will contain a byte/character comprising all zeros at its tail.

appendix b Forward error control

B.1 Introduction

With an automatic repeat request (ARQ) error control scheme, additional check digits are appended to each transmitted message (frame) to enable the receiver to detect when an error is present in a received message, assuming certain types of error. If an error is detected, additional control procedures are used to request another copy of the message. With forward error control (FEC), sufficient additional check digits are added to each transmitted message to enable the receiver not only to detect the presence of one or more errors in a received message but also to locate the position of the error(s). Furthermore, since the message is in a binary form, correction is achieved simply by inverting the bit(s) that have been identified as erroneous.

In practice, the number of additional check digits required for error correction is much larger than that needed for just error detection. In most applications involving terrestrial (land-based) links, ARQ methods similar to those described in Chapter 6 are more efficient than FEC methods, and hence are the most frequently used. Such methods rely on a return path for acknowledgment purposes. However, in most entertainments applications, a return path is simply not available or, even if one was available, the round-trip delay associated with it may be very long compared with the data transmission rate of the link. For example, with many satellite links the propagation delay may be such that several hundred megabits may be transmitted by the sending station before an acknowledgment could be received in the reverse direction. In such applications, FEC methods are used. The aim of this appendix is to give an introduction to the techniques most widely used with FEC methods.

B.2 Block codes

An example of a block code is the Hamming single-bit code. In practice, this FEC method is of limited use for digital transmission. Nevertheless, we shall look at it briefly to introduce the subject of block codes and some of the terms associated with coding theory. Clearly, a comprehensive description of the subject of coding theory is beyond the scope of this book and hence the aim here is simply to give a brief introduction. If you have an interest in coding theory and would like to gain a more extensive coverage, consult some of the references given in the bibliography at the end of the book.

Recall that the term used in coding theory to describe the combined message unit, comprising the useful data bits and the additional check bits, is **codeword**. The minimum number of bit positions in which two valid codewords differ is known as the **Hamming distance** of the code. For example, consider a coding scheme that has seven data bits and a single parity bit per codeword. Assuming even parity is being used, consecutive codewords in this scheme are as follows:

```
0000000  0
0000001  1
0000010  1
0000011  0
```

We can see from this list that such a scheme has a Hamming distance of 2, as each valid codeword differs in at least two bit positions. This means that it does not detect 2-bit errors since the resulting (corrupted) bit pattern will be a different but valid codeword. However, it does detect all single-bit errors since, if a single bit in a codeword is corrupted, an invalid codeword will result.

In general, the error-detecting and error-correcting properties of a coding scheme are both related to its Hamming distance. It can be shown that to detect n errors, we must use a coding scheme with a Hamming distance of $n + 1$, while to correct for n errors, we must use a code with a Hamming distance of $2n + 1$.

The simplest error-correcting coding scheme is the Hamming single-bit code. Such a code detects not only when a single-bit error is present in a received codeword but also the position of the error. The corrected codeword is derived by inverting the identified erroneous bit. This type of code is known as a block code, since the original message to be transmitted is treated as a single block (frame) during the encoding and subsequent decoding processes. In general, with a block code, each block of k source digits is encoded to produce an n-digit block (n greater than k) of output digits. The encoder is said to produce an (n, k) code. The ratio k/n is known as the **code rate** or **code efficiency** while the difference $1 - k/n$ is known as the **redundancy**.

To illustrate this, consider a Hamming code to detect and correct for single-bit errors assuming each codeword contains a 7-bit data field – an ASCII character, for example. Such a coding scheme requires four check bits since, with this scheme, the check bits occupy all bit positions that are powers of 2. This code is known as an (11, 7) block code with a rate of 7/11 and a redundancy of 1 – 7/11. For example, the bit positions of the value 1001101 are as follows:

```
11 10 9 8 7 6 5 4 3 2 1
 1  0 0 x 1 1 0 x 1 x x
```

The four bit positions marked 'x' are used for the check bits, which are derived as follows. The 4-bit binary numbers corresponding to those bit positions with a binary 1 are added together using modulo-2 arithmetic and the four check bits are the following 4-bit sum:

$$\begin{array}{rl} 11 = & 1\,0\,1\,1 \\ 7 = & 0\,1\,1\,1 \\ 6 = & 0\,1\,1\,0 \\ 3 = & \underline{0\,0\,1\,1} \\ = & \underline{1\,0\,0\,1} \end{array}$$

The transmitted codeword is thus:

11	10	9	8	7	6	5	4	3	2	1
1	0	0	*1*	1	1	0	*0*	1	*0*	*1*

Similarly, at the receiver, the 4-bit binary numbers corresponding to those bit positions with a binary 1, including the check bits, are again added together. If no errors have occurred, the modulo-2 sum is zero:

$$\begin{array}{rl} 11 = & 1\,0\,1\,1 \\ 8 = & 1\,0\,0\,0 \\ 7 = & 0\,1\,1\,1 \\ 6 = & 0\,1\,1\,0 \\ 3 = & 0\,0\,1\,1 \\ 1 = & \underline{0\,0\,0\,1} \\ = & \underline{0\,0\,0\,0} \end{array}$$

Now consider a single-bit error: say bit 11 is corrupted from 1 to 0. The new modulo-2 sum is now:

$$\begin{array}{rl} 8 = & 1\,0\,0\,0 \\ 7 = & 0\,1\,1\,1 \\ 6 = & 0\,1\,1\,0 \\ 3 = & 0\,0\,1\,1 \\ 1 = & \underline{0\,0\,0\,1} \\ = & \underline{1\,0\,1\,1} \end{array}$$

Firstly, the sum is nonzero, which indicates an error, and secondly, the modulo-2 sum, equivalent to decimal 11, indicates that bit 11 is the erroneous bit. The latter is inverted to obtain the corrected codeword and hence data bits.

It can also be shown that if two bit errors occur, the modulo-2 sum is nonzero, thus indicating an error, but the positions of the errors cannot be determined from the sum. The Hamming single-bit code can correct for single-bit errors and detect two-bit errors but other multiple-bit errors cannot be detected.

As we saw in Chapter 6, the main types of error in many data communication networks are error bursts rather than, say, isolated single or double-bit errors. Hence, although the Hamming coding scheme in its basic form appears to be inappropriate for use with such networks, a simple technique called interleaving is often used to extend the application of such a scheme.

Consider, for example, a requirement to transmit a block of data, comprising a string of, say, eight ASCII characters, over a simplex channel that has a high probability of an error burst of, say, seven bits. The controlling device first converts each ASCII character into its 11-bit codeword form to give a block of eight 11-bit codewords. Then, instead of transmitting each codeword separately, the controlling device transmits the contents of the block of codewords a column at a time. Thus the eight, say, most significant bits are transmitted first, then the eight next most significant bits and so on, finishing with the eight least significant bits. The controlling device at the receiver then performs the reverse operation, reassembling the transmitted block in memory, prior to performing the detection and, if necessary, correction operation on each codeword.

The effect of this approach is that if an error burst of up to seven bits does occur, it affects only a single bit in each codeword rather than a string of bits in one or two codewords. This means that, assuming just a single error burst in the 88 bits transmitted, the receiver can determine a correct copy of the transmitted block of characters.

Although the approach just outlined provides a way of extending the usefulness of this type of encoding scheme, Hamming codes are used mainly in applications that have isolated single-bit errors; an example is in error-correcting semiconductor memory systems. As we showed in Figure 11.18, the preferred method of achieving FEC in most digital communication systems is based on a combination of a Reed–Solomon block code and a convolutional coder. We shall now briefly describe the operation of convolutional coders.

B.3 Convolutional codes

Block codes are *memoryless* codes as each output codeword depends only on the current *k*-bit message block being encoded. In contrast, with a convolutional code, the continuous stream of source bits is operated upon to produce a continuous stream of output (encoded) bits. Because of the nature of the encoding process, the sequence of source bits is said to be convolved (by applying a specific binary operation on them) to produce the output bit sequence. Also, each bit in the output sequence is dependent not only on the current bit being encoded but also on the previous sequence of source bits, thus implying some form of memory. In practice, as we shall see, this takes the form of a shift register of a finite length, known as the **constraint length**, and the convolution (binary) operation is performed using one or more modulo-2 adders (exclusive-OR gates).

Encoding

An example of a convolutional encoder is shown in Figure B.1(a). With this encoder, the three-bit shift register provides the memory and the two modulo-2 adders the convolution operation. For each bit in the input sequence, two bits are output, one from each of the two modulo-2 adders. The encoder shown is thus known as a rate $1/2(k/n)$ convolutional encoder with a constraint length of 3.

Because of the memory associated with a convolutional encoder, we must have a convenient means of determining the specific output bit sequence generated for a given input sequence. Three techniques can be used, each based on a form of diagrammatic representation: a tree diagram, a state diagram, and a trellis diagram. In practice, the last is the most frequently used method because it is the most useful for demonstrating the decoding operation. However, before we can draw this, we must determine the outputs for each possible input sequence using either the tree or state diagram.

As an example, Figure B.1(b) shows the **tree diagram** for the encoder in Figure B.1(a). The branching points in the tree are known as nodes and the tree shows the two possible branches at each node; the upper of the two branches corresponds to a 0 input bit and the lower branch to a 1 bit. The pair of output bits corresponding to the two possible branches at each node are shown on the outside of each branch line.

As we can see, with a tree diagram the number of branches in the tree doubles for each new input bit. However, the tree is repetitive after the second branch level since, after this level, there are only four unique branch nodes. These are known as *states* and are shown as *A*, *B*, *C*, and *D* in the figure.

As we can see, from any one of these nodes the same pair of output bits and new node state occurs, irrespective of the position of the node in the tree. For example, from any node *C* the same pair of branch alternatives occur: 10 output and new state *A* for a 0 input, or 01 output and new state *B* for a 1 input.

Once we have identified the states for the encoder using the tree diagram, we can draw the **trellis diagram**. As an example, the trellis diagram for the same encoder is shown in Figure B.2(b). As we can see, after the second branch level, the repetitive nature of the tree diagram is exploited by representing all the possible encoder outputs in a more reduced form.

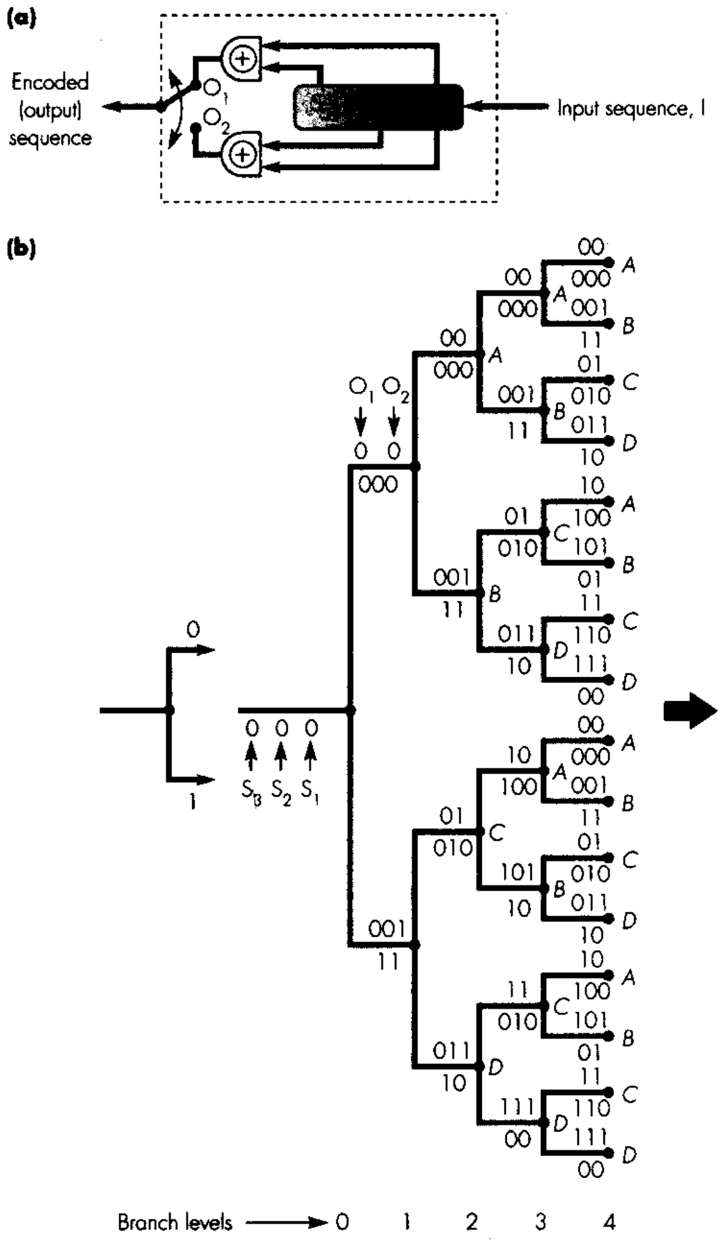
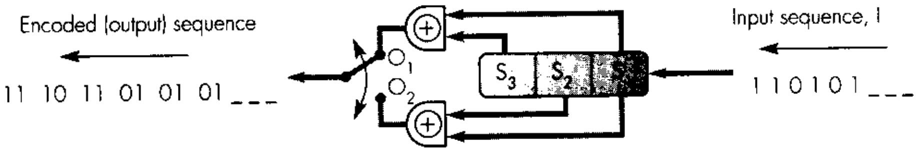


Figure B.1 Convolutional coder principles: (a) example encoder circuit; (b) tree diagram representaton of the encoder.

(a)



Input sequence I	Shift register contents S_1	 S_2	 S_3	Output sequence O_1	 O_2
1	1	0	0	1	1
1	1	1	0	1	0
0	0	1	1	1	1
1	1	0	1	0	1
0	0	1	0	0	1
1	1	0	1	0	1
⋮		⋮		⋮	

(b)

(c)

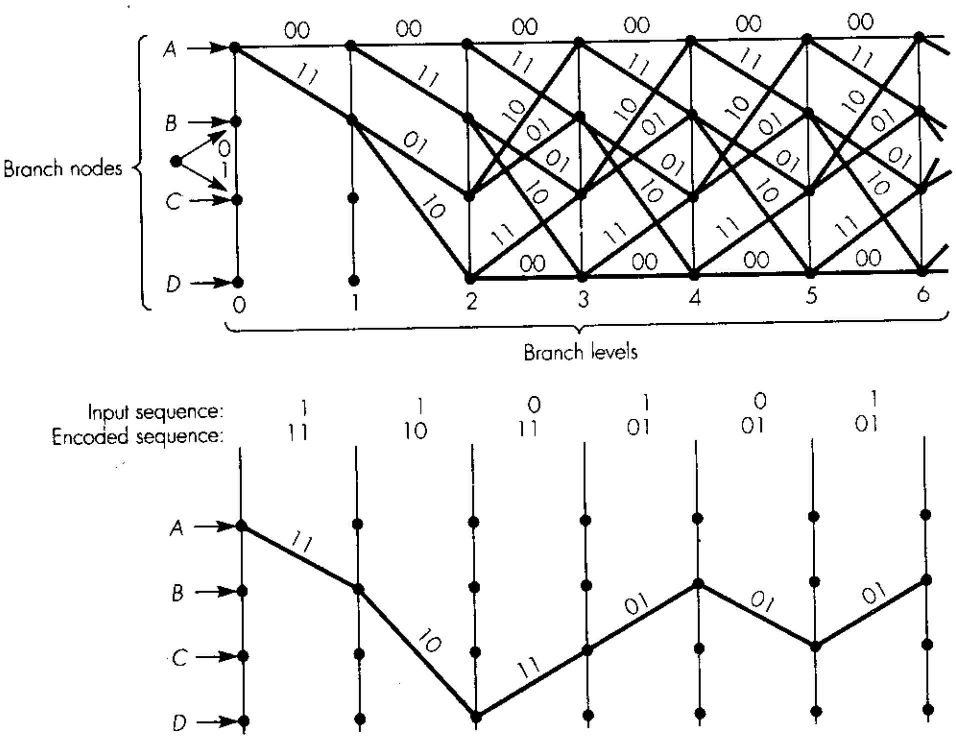


Figure B.2 Convolutional encoder output derivation: (a) circuit; (b) trellis diagram; (c) example output.

The trellis diagram shows the outputs that result from this encoder for all possible input bit sequences. Then, for a specific input sequence, a single path through the trellis – and hence sequence of output bits – results. As an example, Figure B.2(c) shows the path through the trellis, and hence the output sequence, corresponding to the input sequence 110101... .

Initially, we assume that the shift register is cleared, that is, it is set to all 0s. After the first bit in the input sequence has been shifted (entered) into the shift register, its contents are 001. The outputs from the two modulo-2 adders are 0 + 1 = 1 (adder 1) and 0 + 1 = 1 (adder 2). Thus, the first two output bits are 11 and these are output before the next input bit is entered into the shift register. Since the input bit was a 1, the lower branch path on the trellis diagram is followed and the output is 11, as derived.

After the second input bit has been entered, the shift register contains 011. The two adder outputs are 0 + 1 = 1 (adder 1) and 1 + 1 = 0 (adder 2). Thus, the two output bits are 10 and again these are output before the next input bit is processed. Again, since the input bit was a 1, the lower branch on the trellis diagram is followed and the output is 10, as derived. Continuing, the third input bit makes the shift register contents 110 and hence the two output bits are 11; 1 + 0 = 1 (adder 1) and 1 + 0 = 1 (adder 2). Also, since the input bit was a 0, the upper branch path on the trellis diagram is followed. This process then continues.

Decoding

The aim of the decoder is to determine the *most likely* output sequence, given a received bitstream (which may have errors) and a knowledge of the encoder used at the source. The decoding procedure is equivalent to comparing the received sequence with all the possible sequences that may be obtained with the respective encoder and then selecting the sequence that is closest to the received sequence. Recall that the Hamming distance between two codewords is the number of bits that differ between them. Therefore, when selecting the sequence that is closest to the received sequence, the Hamming distance between the received sequence and each of the possible sequences is computed, and the one with the least distance is selected. Clearly, in the limit this necessitates comparing the complete received sequence with all the possible sequences, and hence paths through the trellis. This is impractical in most cases and hence we must compromise.

Essentially, a running count is maintained of the distance between the actual received sequence and each possible sequence but, at each node in the trellis, only a single path is retained. There are always two paths merging at each node and the path selected is the one with the minimum Hamming distance, the other is simply terminated. The retained paths are known as **survivor paths** and the final path selected is the one with a continuous path through the trellis with a minimum aggregate Hamming distance. This procedure is known as the **Viterbi algorithm**. The decoder, which aims to find the most likely path corresponding to the received sequence, is known as a **maximum-likelihood decoder**. Example B.1 describes the Viterbi algorithm.

Example B.1

Assume that a message sequence of 1001110... is to be sent using the encoder shown in Figure B.1(a). From the trellis diagram for this encoder, we can deduce that this will yield a transmitted (output) sequence of:

11 01 10 11 10 00 11 ...

Now assume a burst error occurs so that two bits of this encoded sequence are corrupted during transmission. The received sequence is as follows:

11 01 00 11 11 00 11 ...
↑ ↑

Use the Viterbi algorithm to determine from this the most likely transmitted sequence.

Answer:

The various steps associated with the encoding and decoding procedures are shown in Figure B.3. Part (a) shows the path through the trellis corresponding to the original output from the encoder and part (b) shows how the survivor paths are chosen. The number shown by each path merging at a node in Figure B.3(b) is the accumulated Hamming distance between the path followed to get to that node and the actual received sequence.

If the path chosen is that starting at the root node (branch level 0), the received sequence is 11 and the Hamming distances for the two paths are 2 for path 00 and 0 for path 11. These two distance values are added to the paths emanating from these nodes. Thus, at branch level 1, the received sequence is 01 and the two paths from node *A* have Hamming distances of 1 for path 00 and 1 for path 11. The accumulated distances are thus 2 + 1 = 3 for each path. Similarly, the two paths emanating from node *B* have Hamming distances of 0 for path 01 and 2 for path 10, and hence the accumulated distances are 0 + 0 = 0 and 0 + 2 = 2, respectively. A similar procedure is repeated at branch level 2.

At branch level 3 and onwards, however, the selection process starts. Thus, the two paths merging at node *A* (at branch level 3) have accumulated distances of 3 and 1, of which the latter is selected to be the survivor path for this node – this is shown as a bold line on the trellis diagram. A similar selection process is followed at nodes *B*, *C*, and *D*. At node *C*, however, we can see that the two merging paths both have the same accumulated distance of 4. In such cases, the upper path is selected. Also, after the selection process, all subsequent distances are calculated relative to the accumulated distance associated with the selected path.

▶

B.1 Continued

[illegible] the output [illegible] by inspection [illegible]

- [illegible] trellis;
- [illegible] the minimum.

[illegible] output [illegible] to the origi- [illegible]

Finally, note that no FEC method can identify all errors. In general, codes like the convolutional code are used primarily to reduce the error probability (bit error rate) of a link to a more acceptable level. A typical reduction with a rate 1/2 convolutional coder is between 10^2 and 10^3. Hence when used with a Reed–Solomon (block) coder, the number of residual bit errors after the block decoding process is reduced to a level that is acceptable for most entertainment applications involving audio and video streams.

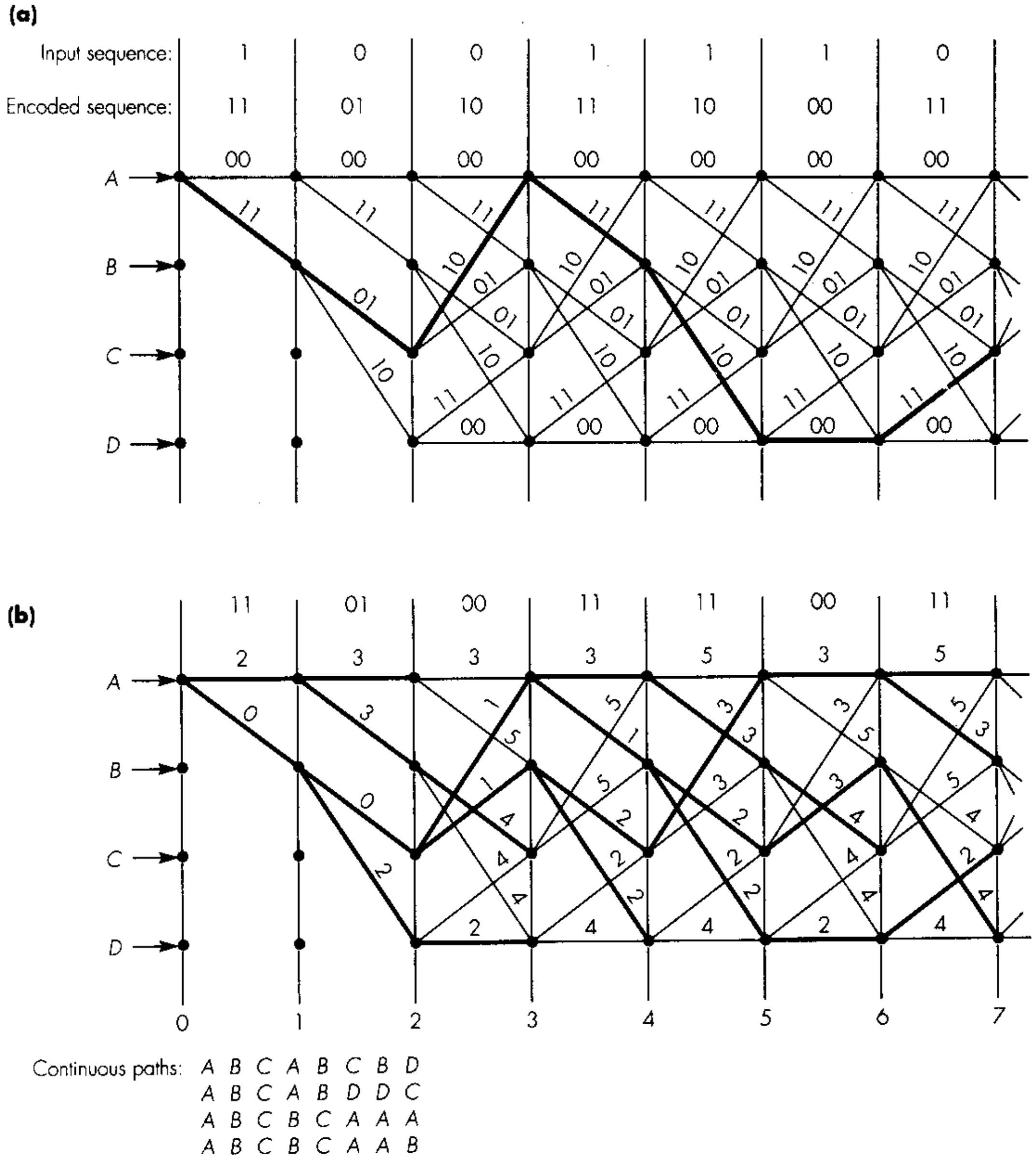


Figure B.3 Convolutional decoder output derivation: (a) actual decoder output; (b) derived survivor paths.

bibliography and further reading

In order to keep abreast of developments in the communications and networking fields, you should try to read on a regular basis the journals and magazines published in these fields by the major institutions. The most widely read journals that contain a range of technical papers in the area of communications and networks are: *IEEE Transactions on Communications, IEEE Journal on Selected Areas in Communications, IEE Proceedings on Communications, Communications of the ACM,* and *Computer Networks and ISDN.* In addition, the IEEE publish four magazines: *IEEE Network, IEEE Communications, IEEE Multimedia,* and *IEEE Internet Computing* all of which contain articles relating to state-of-the-art developments in their related fields.

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